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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/753,766
Filing Date	December 29, 2000
First Named Inventor	Udo Walterscheidt
Art Unit	2183
Examiner Name	Barry J. O'Brien
Total Number of Pages in This Submission: 21	Attorney Docket Number: 42390P10124

ENCLOSURES ***(check all that apply)***

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below):*
  - Check in the amount of $500.00
  - Return Receipt Postcard

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Paul A. Mendonsa, Reg. No. 42,879 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	Paul A Mendonsa
Date	January 11, 2005

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	**Rachael L. Brown**		
Signature	RLB	Date	**January 11, 2005**

Based on PTO/SB/21 (04-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 06/04/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/753,766
Filing Date	December 29, 2000
First Named Inventor	Udo Walterscheidt
Examiner Name	Barry J. O'Brien
Art Unit	2183
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☐ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20. ☒ Credit any overpayments

FEE CALCULATION

1. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	19	- 20* =	0	X	50.00	=	$0.00
Independent Claims	3	- 3* =	0	X	200.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple Dependent claim, if not paid
1204	300	2204	150	**Reissue independent claims over original patent
1205	300	2205	150	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (1) ($) 0.00

***or number previously paid, if greater, For Reissues, see below*

2. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					

SUBTOTAL (2) ($) 500.00

SUBMITTED BY Complete (if applicable)

Name (Print/Type)	Paul A. Mendonsa	Registration No. (Attorney/Agent)	42,879	Telephone	(503) 439-8778
Signature				Date	01/11/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Udo Walterscheidt, et al.

Serial No.:	09/753,766	Group Art Unit:	2183
Filed:	December 29, 2000	Examiner:	B. O'Brien
FOR:	APPARATUS AND METHOD FOR CONCEALING SWITCH LATENCY		

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant submits this appeal brief, thus perfecting the notice of appeal filed on November 12, 2004.

The required headings and subject matter follow.

(i) ***Real party in interest.***

This case is assigned of record to Intel Corporation, who is the real party in interest.

(ii) ***Related appeals and interferences.***

There are no known related appeals and / or interferences.

(iii) ***Status of claims.***

Claims 1-19 are pending in the case and stand rejected. The rejections of claims 1-19 are being appealed.

(iv) ***Status of amendments.***

After the final rejection, an amendment was filed on September 10, 2004. The advisory action mailed October 6, 2004 indicates that the amendment is entered. The attached Claims appendix reflects the current status of amendments.

(v) ***Summary of claimed subject matter.***

Independent claim 1 is directed to a multi-threading processor, including a front end module (page 4, line 12, Fig. 1, front end module 18), an execution module (page 4, lines 12-13, Fig. 1, execution module 20) coupled to the front end module, a state module (page 4, lines 10-12, Fig. 1, state module 12) coupled to the front end module and the execution module, and a switch logic module (page 4, lines 14-15, Fig. 1, switch logic module 22) coupled to the state module, wherein the switch logic module detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of the mispredicted branch. The independent claims 8 and 14 are respectively directed to a method and a set of instructions, including detecting a switching event in a software thread (page 6, line 19, Fig. 3, block 36), determining whether a mispredicted branch has been detected in the software thread (page 6, line 20, Fig. 3, block 38), and executing a switch to another software thread during a latency of the mispredicted branch if the mispredicted branch has been detected (page 6, lines 20-24, Fig. 3, block 40).

(vi) ***Grounds of rejection to be reviewed on appeal.***

I. Claims 1-4, 6-9, and 14-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,933,627 (Parady) in further view of U.S. Patent No. 5,881,277 (Bondi).

II. Claims 5, 10-13 and 16-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Parady, in further view of Brondi, and in further view of U.S. Patent No. 6,567,839 (Borkenhagen).

(vii) ***Argument.***

I. The rejection of claims 1-4, 6-9, and 14-15 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,933,627 (Parady) in further view of U.S. Patent No. 5,881,277 (Bondi), is in error and should be reversed.

Claim 1

With respect to claim 1, the Examiner fails to establish a prima facie case of obviousness. Claim 1 recites, among other things, that the switch logic module detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch. The Examiner admits that Parady fails to teach or suggest this claim recitation on page 3 of the final office action, numbered paragraph 8:

> "8. Parady has not taught that the switch logic detects a mispredicted branch in a thread and schedules a switch to another thread during the latency of the mispredicted branch."

The Examiner further admits that Bondi fails to teach or suggest this claim recitation on page 12 of the final office action at numbered paragraph 41:

> "41. The Applicant is correct in noting that Bondi is directed towards reducing the latency of a mispredicted branch rather than switching to another thread during such latency. ..."

The Examiner incorrectly asserts that applicants are arguing the references individually. In fact, applicants are properly attacking the failed combination and the Examiner's failure to establish a prima facie case of obviousness. It is a basic tenet of the law of obviousness that if a claim recites elements A, B, C, and D, and none of cited references 1 or 2 teaches element D, then the combination of reference 1 and 2 cannot possibly teach or suggest the claimed invention

of elements A, B, C, and D. The Examiner has admitted that neither the Parady reference nor the Bondi reference teaches or suggests the noted claim elements. Therefore, no possible combination of Parady and Bondi can render claim 1 obvious because the admittedly missing claim element is not taught or suggested by the combination. Accordingly, the rejection of claim 1 is in error and should be reversed.

Moreover, claim 1 recites further elements that are missing from both the Parady and Bondi references. In fact, the Examiner completely disregards the structural recitations of claim 1. Specifically, claim 1 recites, among other things, an execution module coupled to said front end module, a state module coupled to said front end module and said execution module, and a switch logic module coupled to said state module emphasis added. Parady fails to teach or suggest these claim recitations. The Examiner relies on components of Parady illustrated in Fig. 3 of Parady for reading on the claim. However, a simple comparison of Fig. 1 of the present specification with Fig. 3 of Parady illustrates that Parady does not teach the structural recitations of claim 1:

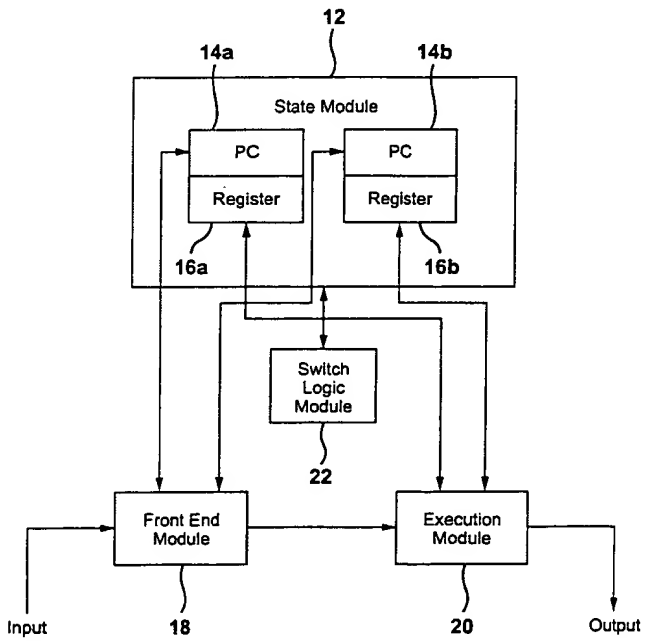

Fig. 1

Present Application

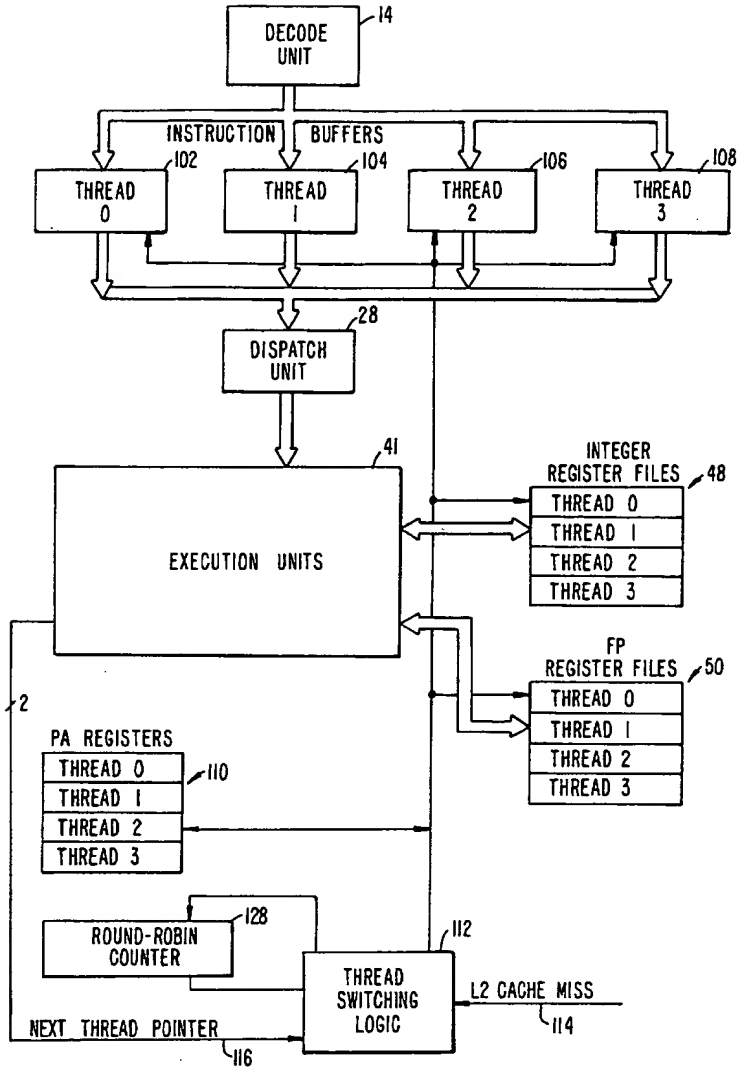

FIG. 3.

Parady

As is apparent from inspection of the above Fig. 3 of Parady, the relied upon decode unit 14 of is not coupled to the relied upon execution unit 41. The office admits that Parady does not teach the recited state module, and instead relies on an improper conflation of components including various register files 48, 50, and 110 as corresponding to the recited state module. However, none of the relied upon components 48, 50, or 110 are coupled to the relied upon decode unit 14.

The Examiner admits on page 9 of the final office action, at numbered paragraph 34, that "the path between the execution module to the front-end module of Parady includes other components ..." The Examiner further admits on page 10 of the final office action, at numbered paragraph 36, that "the path between the register files and PA registers to the front-end module of Parady includes other components ..." However, the Examiner relies on an unreasonably broad interpretation of "comprising" to render any structural recitation in claim 1 meaningless.

In the Examiner's view, apparently, every electronic component in a system is "coupled to" every other electronic component in the system. The Examiner's position is unreasonable and not in keeping with what Parady actually teaches. While "comprising" is open claim language, it does not operate to negate the recited inter-relationship of the claim elements. Particularly from the view of the claim as whole, the structure and inter-relationships of the components in Parady are different from and do not teach or suggest the recited modules and inter-relationship of the modules as recited in claim 1. Accordingly, the rejection of claim 1 is further in error and should be reversed.

The Examiner's analysis is further in error because of an incorrect reading of the Parady reference. The Examiner asserts on page 3 of the final office action, at numbered paragraph 7(d), that Parady teaches a "switch logic module (112 of Fig. 3) coupled to said state module, wherein said switch logic module detects a long-latency event in a software thread and schedules a switch to another thread during a latency of said long-latency event (see Col. 3, lines 57-65)." However, the relied upon thread switching logic 112 does not possess the functionality asserted by the Examiner. For the Board's convenience, the relied upon portion follows:

> "Thread switching logic 112 is provided to give a hardware thread-switching capability. The indication that a thread switch is required is provided on line 114 providing an L2-miss indication from cache control/system interface 22 of Fig. 1. Upon such an indication, a switch to the next thread will be performed, using, in one embodiment, the next thread pointer on line 116. The next thread pointer is 2 bits indicating the next thread from an instruction which caused the cache miss."

The Examiner's analysis fails for several reasons. First, the thread switching logic 112 does not detect the long-latency event, it merely responds to a L2-miss signal. In other words, whatever logic the thread switching logic 112 has, it lacks the logic to detect the event. Instead, it appears that the logic of the thread switching logic 112 is devoted to decoding the next thread. To the extent that the Examiner wishes to broaden his net to catch whatever further logic generated the L2 miss signal, applicants note that such further logic is not coupled to the relied upon state module (i.e. register files 48, 50, and 110).

Moreover, the thread switching logic 112 does not schedule switches, it merely performs them (see above: "Upon such an indication, a switch to the next thread will be performed"). Parady does not teach or suggest that the thread switching logic 112 schedules thread switches or, if it did, that such switches would be scheduled during the latency of the long latency event.

Because the office action's analysis is incorrect, and because Parady fails to teach or suggest even a switch logic module coupled to the state module, wherein the switch logic module detects an event in a software thread and schedules a switch to another software thread during a latency of the event, the office action fails to establish a prima facie case of obviousness. Accordingly, the rejection of claim 1 is further in error and should be reversed.

The rejection further fails because the Examiner has not established proper motivation to modify the Parady reference. The Examiner has admitted on page 10 of the final office action, at numbered paragraph 38, that the "applicant is correct in noting that Parady and Bondi individually do not teach the motivation to combine the references, with Parady being directed towards switching threads on a cache miss, and Bondi being directed towards reducing the latency of a mispredicted branch." Again the Examiner asserts that the applicants are arguing the references individually, when in fact the applicants are attacking the combination. If both references admittedly fail to provide the motivation for the combination, then the motivation must impermissibly come only from the teachings of the present application.

As noted above, the Examiner admits that Parady fails to teach or suggest the recited switch logic module that detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch. In fact, Parady does not even mention and is not concerned with the problem of latency of mispredicted branches. Accordingly, there does not appear to be motivation to modify Parady to address this problem. The final office action clarifies the Examiner's position at page 11, numbered paragraph 39, that Bondi provides motivation to modify Parady because Parady deals with long latency events and Bondi allegedly teaches that mispredicted branches are long latency events. However, the combination still fails to establish a prima facie case of obviousness because even assuming, for the sake of argument, that Bondi provides motivation to modify Parady, Bondi fails to teach or suggest how to modify Parady in a manner that might read on the claims.

As further noted above, the Examiner has admitted that Parady is directed towards switching threads on a cache miss, and that Bondi is directed towards reducing the latency of a mispredicted branch. Assume, for the sake of argument, that one skilled in the art might be motivated to improve the performance of the system in Parady with the teachings of Bondi. Without the benefit of the present application, one skilled in the art would only be motivated to add Bondi's reduced latency mispredicted branches to Parady's system, resulting in a system with both performance improvements. Absent the teachings of the present application, one skilled in the art would not be motivated by Bondi, Parady, or any combination thereof, to modify the thread switching logic 112 of Parady to detect a mispredicted branch in a software thread and schedule a switch to another software thread during a latency of the mispredicted branch.

For any or all of the foregoing reasons, the rejection of claim 1 is in error and should be reversed. Claims 2-7 depend either directly or indirectly from claim 1 and are therefore also patentable.

Claim 2

With respect to claim 2, the office action is incorrect in asserting that the logic 112 detects anything in the software threads. Accordingly, claim 2 is separately patentable.

Claim 3

With respect to claim 3, the office action is incorrect in its assertion. The cited portion is silent with respect to resetting the L2-miss signal when the switch is completed. Accordingly, claim 3 is separately patentable.

Claim 4

With respect to claim 4, the office action admits that the recited outstanding switch request indicator is completely absent from the references, but argues that such a signal must be inherent. This is incorrect. First, although not relevant to the claim, any of a number of mechanisms may be utilized to handle the example given in the office action, none of which are inherent. Accordingly, the recited outstanding switch request indicator is not inherent in Parady. Moreover, as noted above, the logic 112 does not schedule the switches, it merely performs them. Accordingly, it does not teach or suggest the need for an outstanding switch request indicator. Accordingly, claim 4 is separately patentable.

Claims 8 and 14

Applicants strenuously object to the Examiner's characterization of claims 8 and 14 in paragraph 12 of the action as being 'nearly identical' or 'encompassing the same scope' as compared to claim 1. Applicants further objects to similar statements made with respect to other claims throughout the action. Each claim stands on its own and may encompass different and / or broader scope.

With respect to claims 8 and 14, the Examiner fails to comply with 37 C.F.R. § 1.104 (c)(2) because the Examiner fails to sufficiently designate the particular part of each reference relied upon for disclosing each claim recitation, so that a full and fair analysis and response may be made. In fact, the office action fails completely to establish how the references might be read on the claims. Claims 8 and 14 each recite:

detecting a switching event in a software thread;

determining whether a mispredicted branch has been detected in said software thread; and

executing a switch to another software thread during a latency of said mispredicted branch if said mispredicted branch has been detected.

Even upon casual inspection it is apparent that the scope of claim 1 and claims 8 and 14 are not 'nearly identical'. Applicants cannot fairly respond to a rejection that has not been articulated. In any event, the Examiner has not met his burden. In particular, the Examiner has failed to identify what portion(s) of the references are relied upon for teaching detecting a switching event in a software thread and determining whether a mispredicted branch has been detected in said software thread.

In the absence of a legally sufficient rejection, the office action fails to establish a prima facie case of obviousness with respect to claims 8 and 14, and claims 8 and 14 are patentable over the cited combination of references. The respective dependent claims 9-13 and 15-19 are likewise patentable.

Applicants further note, out of an abundance of caution, that for at least the reasons given above with respect to claim 1, neither Parady nor Bondi teaches or suggests executing a switch to another software thread during a latency of a mispredicted branch if the mispredicted branch has been detected. Accordingly, independent claims 8 and 14, and their respective dependent claims are patentable over Parady in view of Bondi.

II. The rejection of claims 5, 10-13 and 16-19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Parady, in further view of Brondi, and in further view of U.S. Patent No. 6,567,839 (Borkenhagen), is in error and should be reversed.

Borkenhagen, which is relied upon for various teachings admitted to be missing from Parady and Brondi, fails to make up for the above noted deficiencies with the Parady and Bondi references. Accordingly, the office action fails to establish a prima facie case of obviousness with respect to the rejected claims.

CONCLUSION

In view of the foregoing, favorable reconsideration and reversal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner and / or the Board is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

January 6, 2005
Date

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on:

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Rachael Brown
Name of Person Mailing Correspondence

Signature

1-11-05
Date

(viii) ***Claims appendix.***

1. A multi-threading processor, comprising:

a front end module;

an execution module coupled to said front end module;

a state module coupled to said front end module and said execution module; and

a switch logic module coupled to said state module, wherein said switch logic module detects a mispredicted branch in a software thread and schedules a switch to another software thread during a latency of said mispredicted branch.

2. A multi-threading processor as recited in claim 1, wherein the switch logic module detects a switching event.

3. A multi-threading processor as recited in claim 2, wherein the switch logic module includes a mispredicted indicator that is set when a mispredicted branch is detected and reset when the switch is completed.

4. A multi-threading processor as recited in claim 3, wherein the switch logic module includes an outstanding switch request indicator that is set when the switching event does not require an immediate switch.

5. A multi-threading processor as recited in claim 4, wherein the switch logic module includes a counter to schedule a switch based on a time quantum.

6. A multi-threading processor as recited in claim 1, wherein the state module includes a pair of register files and a pair of instruction pointers.

7. A multi-threading processor as recited in claim 6, wherein the instruction pointers are coupled to the front end module and the register files are coupled to the execution module.

8. A method for concealing switch latency in a multi-threading processor, comprising:

detecting a switching event in a software thread;

determining whether a mispredicted branch has been detected in said software thread; and

executing a switch to another software thread during a latency of said mispredicted branch if said mispredicted branch has been detected.

9. A method for concealing switch latency in a multi-threading processor as recited in claim 8, further comprising executing a switch to another software thread if the switching event requires an immediate switch.

10. A method for concealing switch latency in a multi-threading processor as recited in claim 9, further comprising ensuring that the switch to another software thread is executed before a time quantum expires.

11. A method for concealing switch latency in a multi-threading processor as recited in claim 10, wherein the switch has a latency of about 15 to about 20 clocks.

12. A method for concealing switch latency in a multi-threading processor as recited in claim 11, wherein the time quantum is less than about 1,000 clocks.

13. A method for concealing switch latency in a multi-threading processor as recited in claim 12, wherein the time quantum is about 200 clocks.

14. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a processor for concealing switch latency in a multi-threading processor comprising:

detecting a switching event in a software thread;

determining whether a mispredicted branch has been detected in said software thread; and

executing a switch to another software thread during a latency of said mispredicted branch if said mispredicted branch has been detected.

15. The set of instructions as recited in claim 14, further comprising executing a switch to another software thread if the switching event requires an immediate switch.

16. The set of instructions as recited in claim 15, further comprising ensuring that the switch to another software thread is executed before a time quantum expires.

17. The set of instructions as recited in claim 16, wherein the switch has a latency of about 15 to about 20 clocks.

18. The set of instructions as recited in claim 17, wherein the time quantum is less than about 1,000 clocks.

19. The set of instructions as recited in claim 18, wherein the time quantum is about 200 clocks.

(ix) ***Evidence appendix.***

None.

(x) ***Related proceedings appendix.***

None.